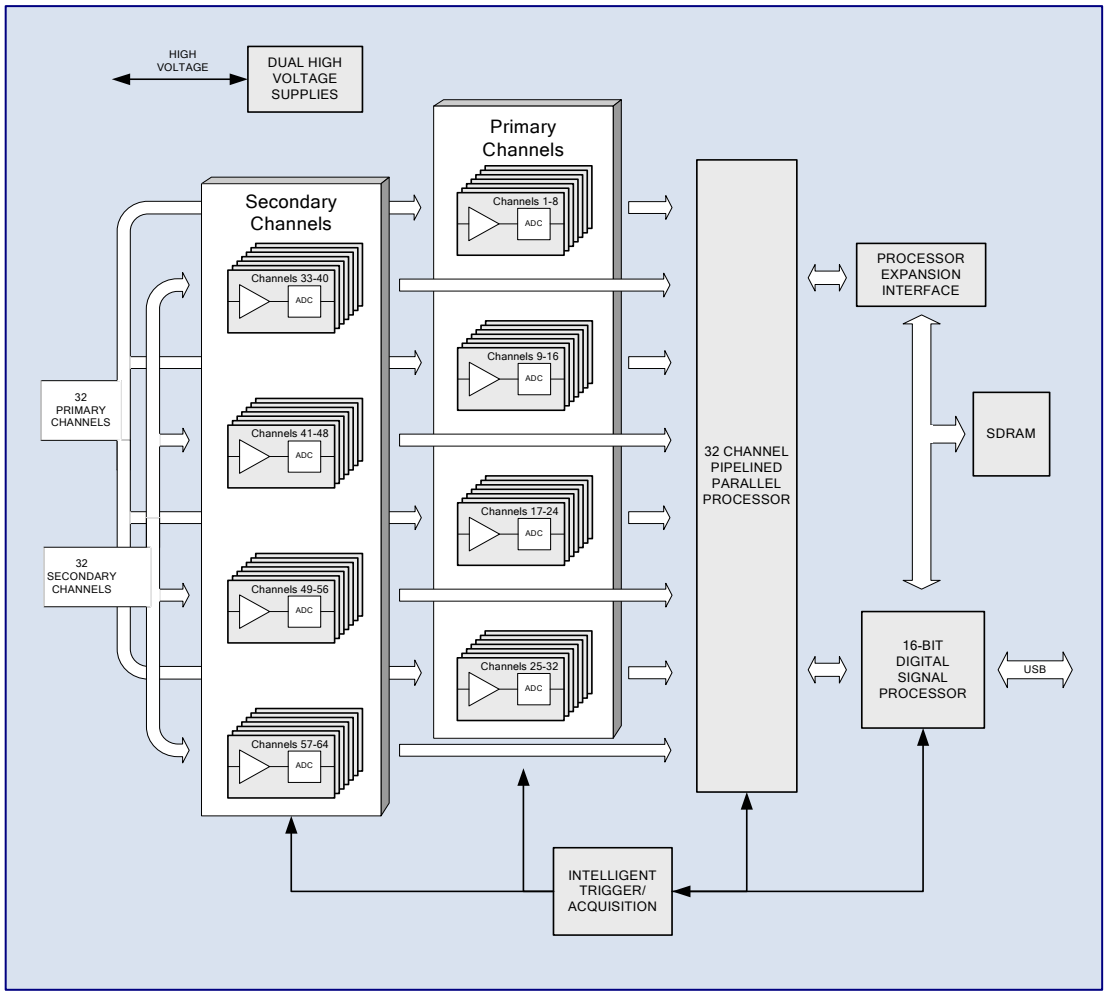
PhotoniQ: Data Processing Architecture

Application Note

The PhotoniQ models IQSP480 and IQSP580 consist of 32 input channels made up from four independent banks of eight charge collection and data acquisition channels. Models IQSP482 and IQSP582 consist of 64 input channels made up from four independent banks of sixteen charge collection and data acquisition channels. Each bank is independently configured and triggered and generates eight parallel streams of digital data as shown in the figure below. The dynamic range and acquisition speed is dependent on the model number — the IQSP480 and IQSP482 having the higher dynamic range and the IQSP580 and IQSP582 having the higher speed. The intelligent trigger/ acquisition module configures the triggering and acquisition parameters for each bank such that any one of multiple triggering modes can be used to initiate the data acquisition process. Thirty-two parallel digital data channels are output to the Pipelined Parallel Processor (P3) where it performs data discrimination and channel uniformity correction. The resulting data is sent to the DSP where it is packetized and sent to the USB output port. Additional reserved DSP processing power can be used to implement user defined filter, trigger, and data discrimination functions.



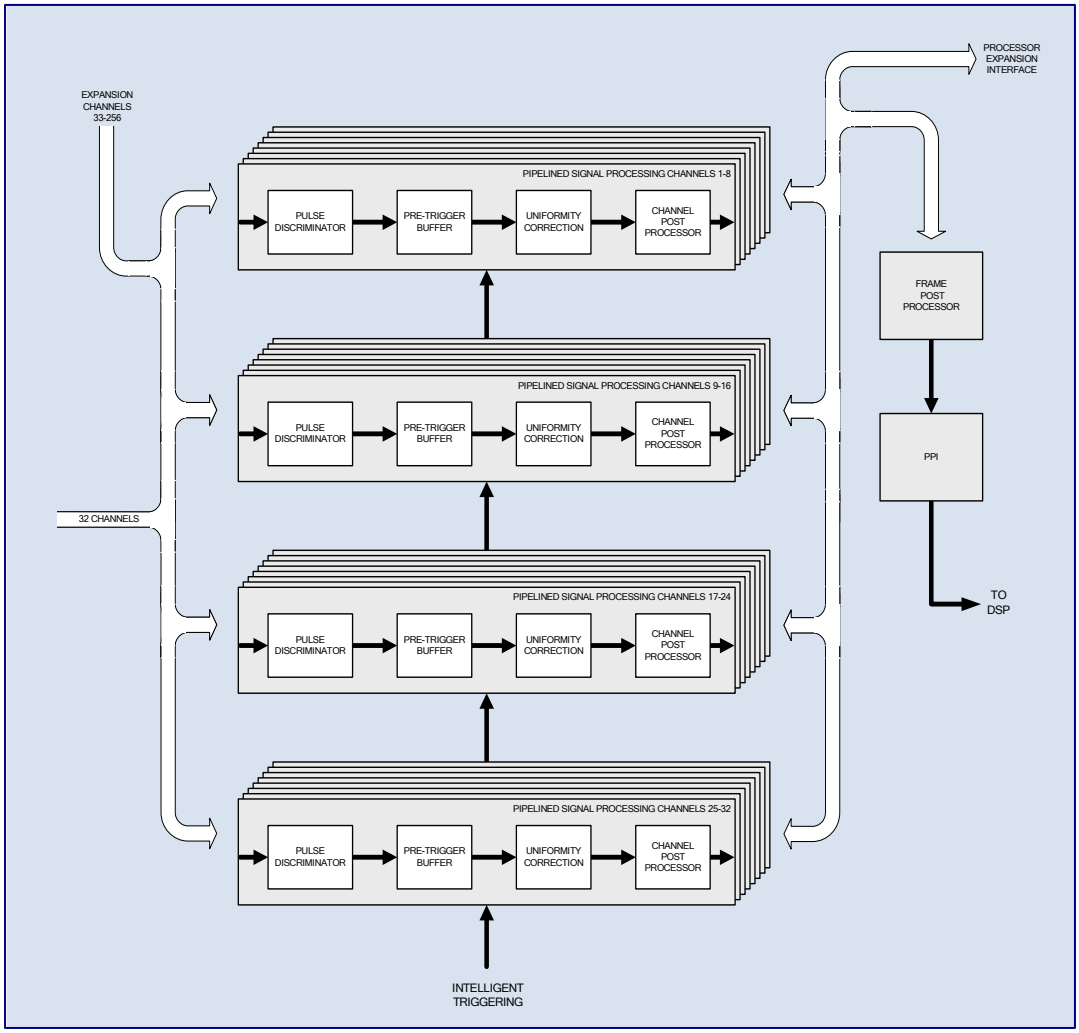
PhotoniQ Functional Block Diagram

Charge Collection & Data Acquisition Channels

Data acquisition is initiated by a trigger event detected by the PhotoniQ's intelligent trigger module. Each trigger starts the collection and digitization of charge signals from the PMT or photodiode sensors across all channels. This functionality, which is shown in the previous figure as an amplifier followed by an ADC, is implemented primarily as precision analog circuit elements that integrate, amplify, and digitize charge. The parallel architecture of this circuitry allows charge integration and digitization to take place simultaneously across all channels thus achieving very high data acquisition speeds. Additionally, the proprietary design of the front end preamp permits very narrow charge pulses to be reliably captured with single photon sensitivity at very high repetition rates.

Pipelined Parallel Processor

The P3 Pipelined Parallel Processor is a dedicated high speed hardware processing unit that executes 32 parallel channels of computations on the 32 data streams from the front-end digitizing blocks. Each channel processor performs real-time data discrimination, buffering, and channel uniformity correction. The outputs from the 32 channel processors are sent to the frame post processor where additional frame-formatted data manipulation is performed. The frame post processor output is sent to the Parallel Peripheral Interface (PPI) where it is formatted and transferred to the DSP for further processing.



32-Channel Pipelined Parallel Processor

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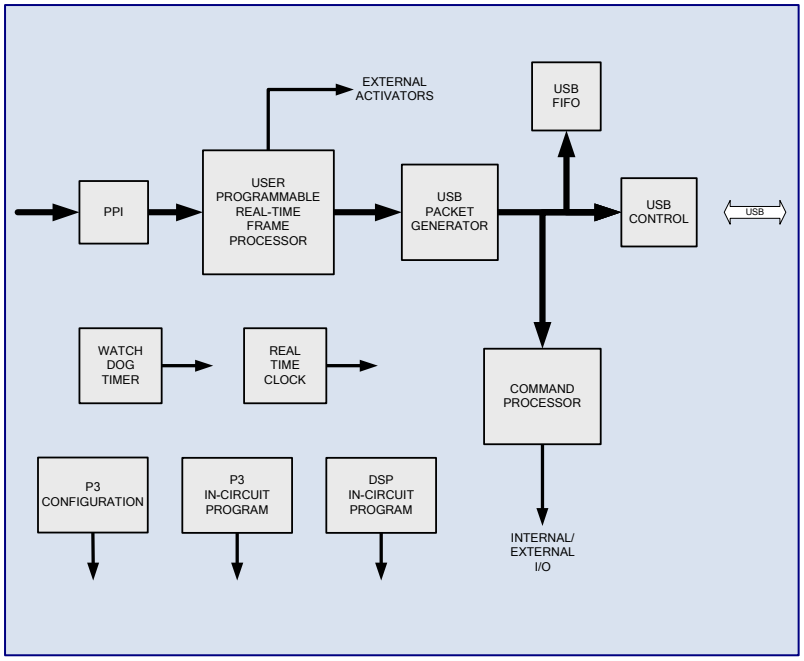
Digital Signal Processor



The 16 bit fixed point digital signal processor performs the high level data manipulation and system control in the PhotoniQ. Channel data received from the P3 on the PPI is routed through the DSP and buffered using the on-board SDRAM. This architecture allows the PhotoniQ to capture very large frames of data, such as the kind typically found in imaging applications, without the loss of any data. Once the data is stored, it is packetized by the USB packet generator and sent out to the PC through the USB 2.0 port. Extra computational power is reserved in the DSP so that user-defined algorithms can be executed on the data prior to transmission. This has the benefit that routines that were previously performed off-line by the PC can instead be handled in real-time. The net effect is that the downstream data load to the PC is reduced so that throughput can be increased by orders of magnitude. In addition to user-defined filtering and triggering functions, the DSP can be used to process commands from the PC and drive external actuators and devices.

Control and Acquisition Interface Software

The PhotoniQ is programmed and monitored by the Control and Acquisition Interface Software. This software, which is resident on the PC, provides a convenient GUI to configure and monitor the operation of the unit. Configuration data used to control various functions and variables within the PhotoniQ such as trigger and acquisition modes, integration time, processing functions, etc. is input through this interface. For custom user applications, the GUI is bypassed and control and acquisition is handled by the user's software that calls the DLLs supplied with the PhotoniQ. As configuration data is modified, the PhotoniQ's local, volatile RAM memory is updated with new configuration data. The hardware operates based upon the configuration data stored in its local RAM memory. If power is removed from the PhotoniQ, the configuration data must be reprogrammed through the GUI. However, a configuration can be saved within the non-volatile flash memory of the PhotoniQ. At power-up, the hardware loads configuration data from its flash memory into its volatile RAM memory. Alternatively, the RAM memory can be configured from a file on the user's PC.

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AN3317.1.3 Jul 2007

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